Amendments to the Specification:

Please replace the title of the specification with the following amended title:

[Method of Producing a] SI-GE Base Heterojunction Bipolar Device

Please replace the Abstract of the application with the following amended Abstract:

A bipolar transistor is disclosed that is produced using a [method of producing a bipolar transistor includes the step of providing a] sacrificial mesa disposed over a layer of SiGe in order to prevent a polysilicon covering layer from forming over a predetermined region of the SiGe layer forming the transistor base. After an etching process, [removes] the sacrificial mesa is removed and the SiGe layer is exposed, where an oppositely doped material is applied over top of the SiGe layer to form an emitter. This makes it possible to realize a thin layer of silicon germanium to serve as the transistor base. The transistor device formed using the sacrificial mesa results in [This method prevents] the base layer SiGe from being affected, as it otherwise would be using a conventional double-poly process, which results in a more repeatable bipolar transistor device yield.

Please replace paragraphs 0040, 0041, 0042, 0052, 0053, 0062 and 0063 of the application currently on file with the following paragraphs 0040, 0041, 0042, 0052, 0053, 0062 and 0063:

[0040] Figs. 3a through 13 are cross-sectional views of schematic representations of a structure illustrating various process to produce a "double poly" SiGe heterojunction bipolar transistor (HBT) in accordance with this invention;

[0041] More particularly Fig. 3a illustrates a portion of a pre-treated silicon wafer in condition to accept a layer of SiGe and a layer of Si in a region for forming a transistor;

[0042] Figs. [3a and 3b] 3b and 3c illustrate the process of depositing a nucleation layer in accordance with an aspect of this invention;

[0052] Figs. 3a through 13 illustrate sequential steps in the formation of a bipolar junction transistor starting with a silicon wafer. Figs 14 through 24 illustrate same sequential steps for the formation of a BJT wherein the layers formed are planar.

[0053] [In] Referring to Fig. 3a a silicon wafer is shown, serving as both a substrate 110 and collector of a bipolar junction transistor. The silicon substrate 110 has a region of n^+ doped material buried within the substrate providing as a low resistance sub-collector. The following process steps will illustrate the formation of a base and emitter, wherein the base of the transistor is grown over a region of the substrate 110. Regions 102 of field oxide SiO_2 are disposed over the silicon, providing insulating regions. A thin 100-800 Å layer 101 of poly-silicon is deposited over a portion of the field oxide regions 102 and over a small region of the window of silicon 110 between the two field oxide regions 102 shown, which serve as a sacrificial material to minimize loading effects and which minimize the effect of moisture within SiO_2 regions 102. The thin poly-silicon layer 101 also provides a surface upon which a layer of SiGe will adhere, and forms an electrical contact to the SiGe layer.

[0062] An essential step in a manufacturable epitaxial process is the reproducible deposition of epitaxial silicon and/or SiGe on a mixed topography i.e. single crystal silicon, poly Si, and oxide (or nitride) of variable roughness. This invention discloses a method for deposition of a seed layer atop the collector region to form a planar surface and a thin uniform thickness, continuous interconnecting silicon or silicon germanium layer without pinholes and defect free. The term thickness is understood by those of skill in the art as a thickness of a layer in a direction perpendicular to a plane of a surface of a wafer on which the layer is formed. Turning now to [Figs. 3a and 3b] Figs. 3b and 3c a preferred embodiment of the invention is shown wherein a nucleation seed layer of Si or SiGe is applied over a mixed topology of layers shown, comprising poly-silicon 101, a section 103 of the region 102 of SiO_2, and the silicon substrate 110. This is accomplished at ultra low pressure and ultra-low flow rates to provide adequate time for nucleation of the deposited layer on all surfaces; oxide, nitride, polysilicon, epitaxial silicon and SiGe. Smooth deposited layers of uniform thickness with continuous coverage of all surfaces is

possible using this method. In order to have the continuous film or seed layer deposit and nucleate over the entire region of the dissimilar materials such as dielectric material and semiconductor material, it is important to meet several conditions. Deposition must be performed at a low temperature below 600 °C, a low pressure of less than 10^{-2} mbar, and at low flow rate of less than 5 cm^3/min. Another advantage to this method, is that in a mixed topography wherein relatively different sized Si and oxide regions exist, by depositing a seed layer in accordance with the teachings of this invention over top of these regions, at low temperature, pressure and flow rate, loading effects are substantially minimized when the SiGe layer is deposited upon the seed layer. Seed layers have been discussed in the prior art, however these layers have not achieved a desired effect of nucleating a continuous film over a large region of dissimilar materials including dielectrics and semiconductors. Furthermore, prior art seed layers are applied at higher temperatures, flow rates and pressure than are taught in this invention in order to increase the throughput. Surprisingly, it was discovered by the inventors of this invention, that lowering the temperature, pressure and flow rate allowed nucleation that would not otherwise occur. Without the seed layer no deposition on oxide or nitride surfaces is possible thereby resulting in a discontinuous film of silicon or SiGe over mixed surface topography which would substantially increase R_b. Planarization of the prior surfaces reduces roughness and removes prior process deficiencies. Residual patches of silicon dioxide or carbon-containing material on the exposed silicon window surface can result in defects during post epitaxy processing by injecting dislocations and other defects such as stacking faults. The seed layer drastically reduces this tendency by introducing a planar surface coverage thereby removing the stress concentration at any heterogeneity in the interface and at discontinuities in the surface, for example silicon/silicon dioxide/poly silicon.

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[0063] The method of providing the seed layer will now be described in accordance with a preferred embodiment of the invention. Prior to introduction into the UHVCVD system all surfaces of the wafer are cleaned using standard RCA[*] cleaning procedures and dipped to hydrophobicity in a 10:1 diluted HF:H2O to ensure removal of contamination

debris from processing and residual native oxide from silicon rich surfaces. The UHVCVD system and its operation are described elsewhere[*]. Immediately on insertion of the wafers into the growth chamber under a flow of preferably less than 500 sccm of hydrogen, silane at the reduced flow rate of less than 20 sccm is injected into the deposition chamber to initiate the nucleation of silicon and produce the seed layer on all exposed surfaces. The seed layer has a thickness for conformal nucleation of Si from silane. Preferably, the thickness of the "nucleation layer" is a minimum of 2 nm and is optimized for a specific mixed topography in the range of 2 to 20 nm is and can be doped or undoped with impurities such as B or P, p- or n-type.

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